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Patents List (Differential Signal Balancer)

Title of invention	Abstract	Country	Filing Date	lssue Data	Effective Date	Patent NO	US Publish	WO Publish
Electromagnetic delay line inductance element	[PROBLEMS] To provide a concentrated constant type electromagnetic delay line inductance element which can easily be made as an ultra-small chip shape and obtain a preferable connection state at each interval. [MEANS FOR SOLVING PROBLEMS] Spriar-shaped inductors L08, L4A, L4B are formed on a first insulating substrate (15) and the inductor L4A is connected in series to the inductor L4B. Spiral-shaped inductors L2A, L2B, L6A are formed on a second and a third insulating substrate (24, 33). Spiral-shaped inductors L2A, L2B, L6A are formed on a fourth insulating substrate (14) and the inductor L2A is connected in series to the inductor L2B. The first to the fourth insulating substrates (15-41) are stacked on one another and the inductors L4D to L6A are connected in the longitudinal direction. The inductors L2A and L2B and the inductors L4A and L4B are divided into two portions in the horizontal direction so as to form one interval and positively connected to the preceding and the following interval not divided in the horizontal direction.	Japan	2004/11/2	2009/11/18	2024/11/2	JP4368352(B2)	US2007/0035363 A1	WO2005043750 (A1)
Common mode filter	To pass an ultra high-speed differential signal and make it difficult to pass a common mode noise. Lumped—constant differential delay line DL is formed by arranging inductors Lo, being passive series elements, and capacitors Co, being passive parallel elements, in a differential four terminal network of a ladder shape composed of the passive series elements and the passive parallel elements arranged in differential lines 1 and 3. The lumped-constant differential delay line DL is composed of capacitors Co including two capacitors Co/2 and Co/2, or Co and Co equivalent to the aforementioned capacitors, having equal values, and connected in series. Inductors L1 to L4 for attenuating a common mode noise are connected between connection points of the capacitors Co/2 and Co/2 or Co and Co connected in series, and a ground potential, so that attenuation poles are formed for attenuating the common mode noise together with the capacitors Co/2 and Co.	Japan	2009/9/25	2013/11/27	2029/9/25	JP5352881(B2)		
		USA	2010/9/17	2014/10/21	2030/9/16	US8866566 (B2)		
		EU	2010/9/24	2015/4/22	2030/9/23	EP2302793 (B1)		
		China	2010/9/21	2014/8/13	2030/9/20	CN102035490 (B)		
Common mode filter	There is provided a common mode filter capable of allowing an ultrahigh speed differential signal to transmit and hardly allowing a common mode noise to transmit, comprising: a lumped-constant differential delay line DL formed by arranging inductors Lo, being passive series elements, and capacitors Co, being passive parallel elements, in a ladder-shaped differential four terminal network composed of the passive series elements and the passive parallel elements arranged in the differential lines 1,3. In the lumped-constant differential delay line DL, the capacitors Co, being pasalter series elements are formed of two capacitors connected in series equivalent to each other and having same values with each other such as Co/2 and Co/2, or Co and Co. Inductors L1 to L4 and resistors R1 to R4 for attenuating the common mode noise are connected between connection points T1 to T4 of the capacitors Co/2 or Co connect in series and a ground potential, thus forming a common mode noise attenuating series resonance circuit together with the capacitors Co/2, Co.	Japan	(2009/11/2)	2013/11/13	2030/10/13	JP5341201 (B2)		
		USA	2010/10/13 ★	2014/9/30	2030/9/16	US8847705 (B2)		
		China	2010/10/13 ★	2015/6/10	2030/10/12	CN102474235 (B)		
Common mode filter	In an ultrahigh-speed differential transmission line, an ultrahigh-speed differential signal is passed to sufficiently attenuate a common mode signal. A pair of conductor paths (1A, 1B) are formed on one side surface of a dielectric layer (3) in parallel. A floating ground (5) is formed on the other side surface of the dielectric layer (3) so as to face the conductor paths (1A, 1B). The floating ground (5) is not connected to a common ground (7) outside and is independent therefrom. A passive two- terminal circuit (CM1) consisting of a passive circuit element is connected between a connection point (9) of the floating ground (5) and the common ground (7).	Japan	2009/7/7 ★	2014/1/22	2029/7/7	JP5393786 (B2)	US2012098627 (A1)	
		China	2009/7/7 ★	2015/3/18	2029/7/6	CN102577116 (B)		
Common mode filter	To sufficiently attenuate a common mode signal by passing an ultra-high speed differential signal through an ultra-high speed differential transmission line. A common mode filter comprises: a pair of conductive lines formed on a first dielectric layer to transmit a differential signal; a plurality of first divided floating grounds in a state of being separated from an external ground potential, and facing the conductive lines, with the first dielectric layer interposed between them, and formed by being divided into a plurality of numbers in a length direction of the conductive lines, and forming a distribution constant type differential transmission line for the differential signal, together with the conductive lines;; and a first passive two-terminal network connected between the first divided floating grounds is least at an input side or an output side of the first divided floating grounds, and the external ground potential.	Japan	(2009/7/27)	2013/10/11	2029/7/26	JP5386586 (B2)		
		USA	2010/7/21 ★	2014/12/30	2030/7/20	US8922303 (B2)		
		China	2010/7/21 ★	2014/9/3	2030/7/20	CN102422533 (B)		

Differential Signal Balancer (DSB) CDLD/CDLA Type

Improving P/N balance in the differential transmission line, absorbing common-mode noise in Ultra-High speed differential transmission line

Appearance forms



Non-Magnetic materials applied products by Delay Line Technology
Available for 10 ~ 28 Gbit/s transmission speed
Improving P/N Line Balance in Differential Signal

Absorbing radiative common-mode noise over GHz range

Example (1) Common-mode Removal (25 Gb/s) Structure

CDLA 1.2 mm × 1 mm



H: 2 GHz/div, V: 1 mV/div





■ Example (2) Smaller Reflection than CMC (Common-mode Choke Coil) Affection of Impedance Mismatch in 10 Gb/s, USB Type-C, 0.5 m Cable Transmission



■Example (3) 25 Gb/s PAM4 (6.25 GHz Clock) with Skew

ELMEC Corporation

URL:http://www.elmec.co.jp



About ELMEC Corporation

ELMEC Corp. is a world-wide leader in the industry of super-high speed passive comporments. Since 1981, ELMEC has kept the top supplier of Delay Lines, and M. Kameya (President/CEO) invents DSBs. ELMEC owns 10+ patents of DSB (Japan and International).